Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1A**
2. **1Y**
3. **1Z**
4. **E1, 2**
5. **2Z**
6. **2Y**
7. **2A**
8. **GND**
9. **3A**
10. **3Y**
11. **3Z**
12. **E3, 4**
13. **4Z**
14. **4Y**
15. **4A**
16. **VCC**

**.090”**

**.129”**

**M174Y**

**MASK**

**REF**

**14 13 12 11 10**

**2 3 4 5 6**

**15**

**16**

**17**

**9**

**8**

**7**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: M174Y**

**APPROVED BY: DK DIE SIZE .099” X .129” DATE: 1/24/23**

**MFG: NATIONAL THICKNESS .014” P/N: 96F174**

**DG 10.1.2**

#### Rev B, 7/1